

Your Manufacturer Is Stupid

Help Them



Chris Denney

CTO - Worthington Assembly



Chris Denney



Chris Denney

Jerk Who Tells You There's A Problem



Your Manufacturer Is Stupid

Have to act stupid



Your Manufacturer Is Stupid

Play dumb on new products





Information about your design is unclear

Phone calls needs to be made



The Problem



I hate people calling me. I hate calling people.

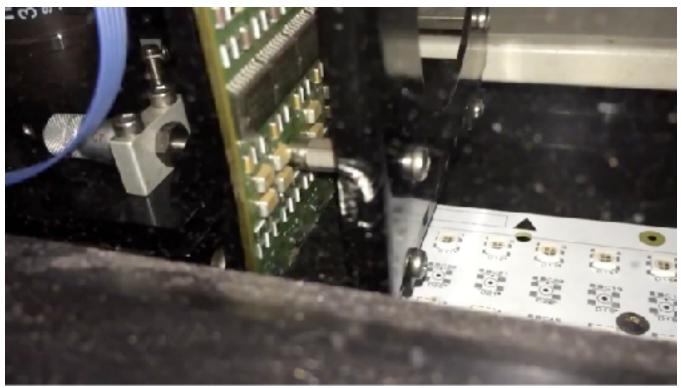




The Problem

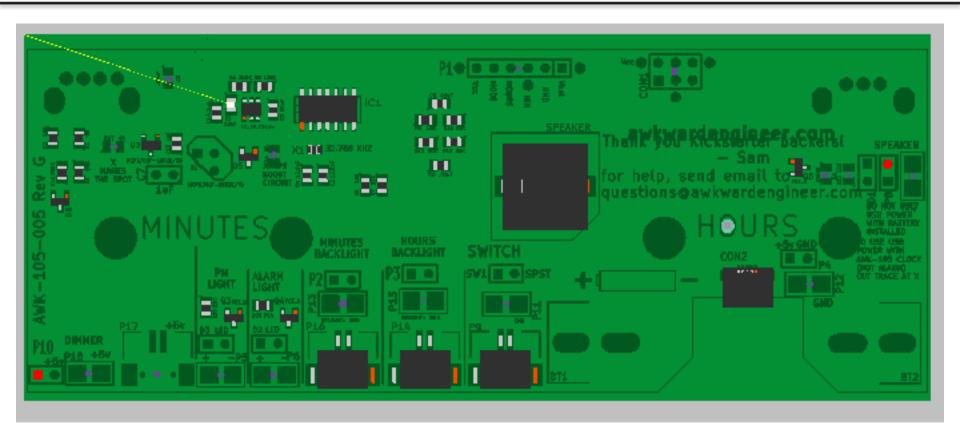


But machines build things!





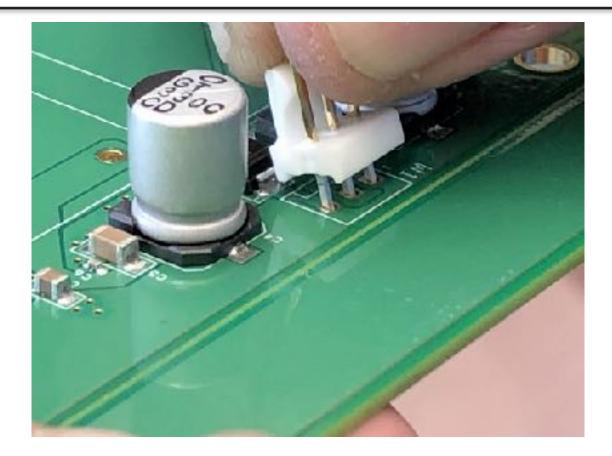
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Actually, humans build things

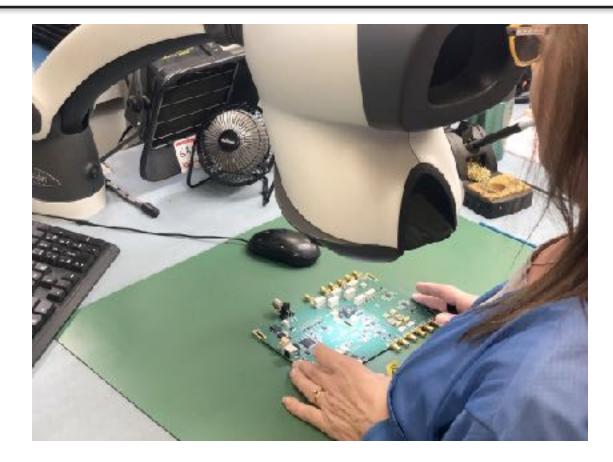
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Actually, humans build things









- 1. Identifying polarity of components
- 2.Silkscreen legibility
- **3.**Panelization
- 4.PCB properties
- 5. Specific manufacturer's part numbers





- 1.Identifying polarity of components
- 2.Silkscreen legibility
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The number 1 problem

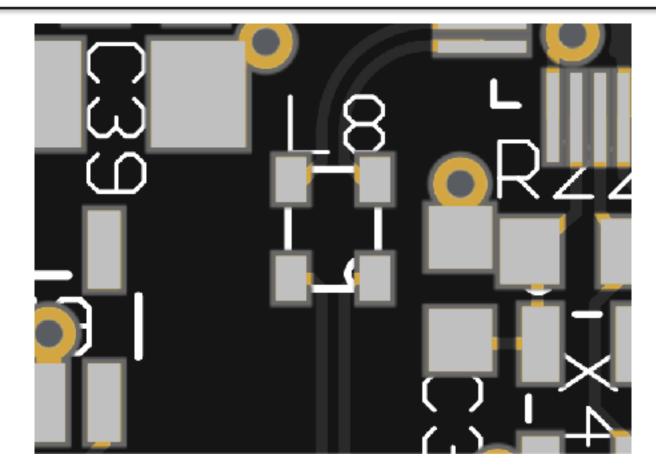




- Polarity of all IC's
 - What is this IC's reference designator?
 - Which pad is Pin 1
- Polarity of all diodes
- Polarity of all LED's
 - This LED here, what reference designator is it?
 - Which pad is the cathode?

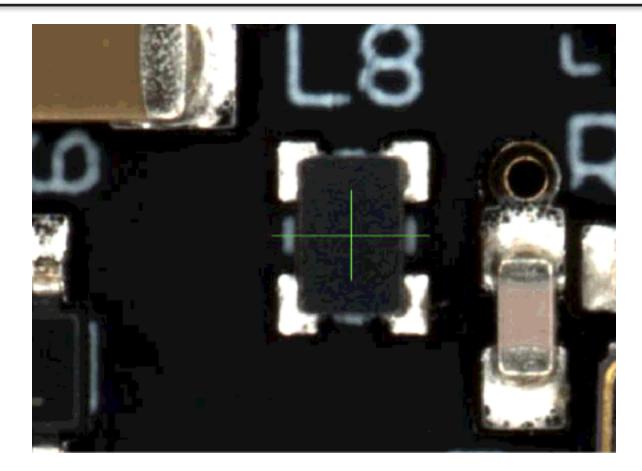






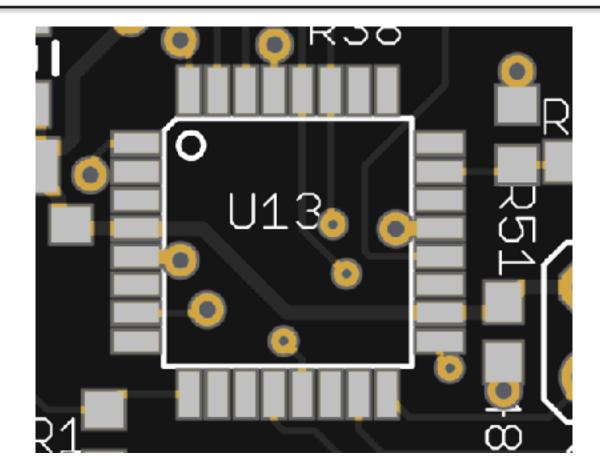






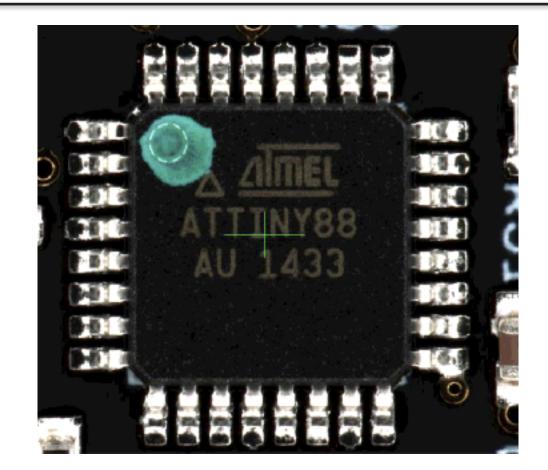






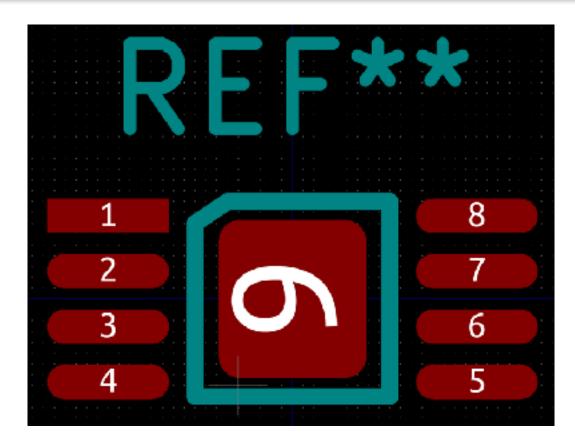






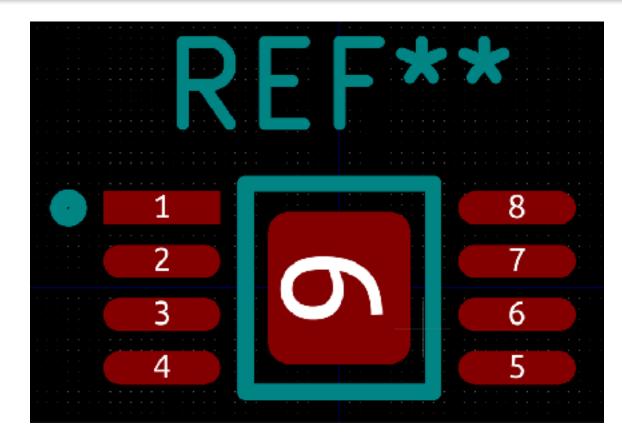






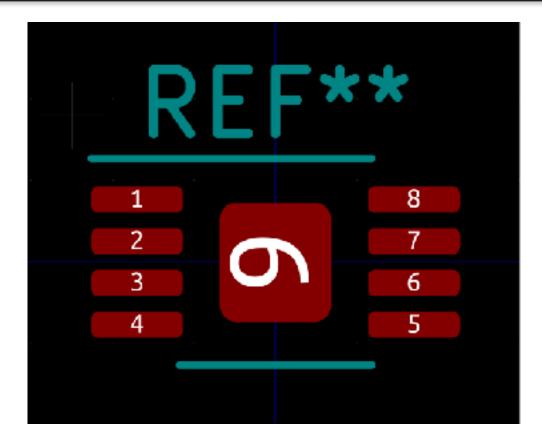
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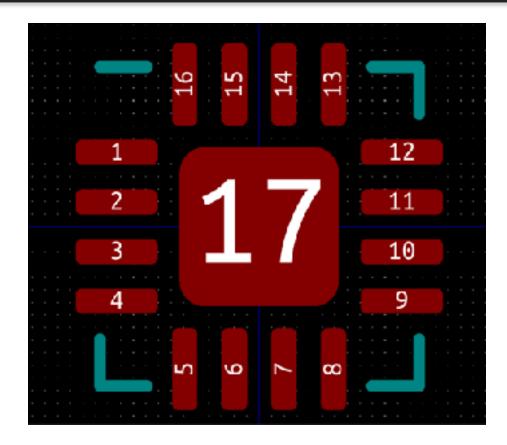


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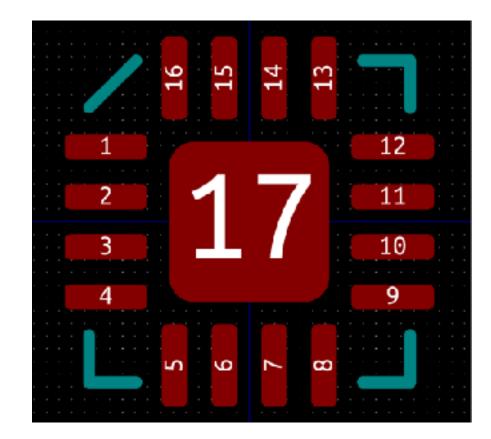








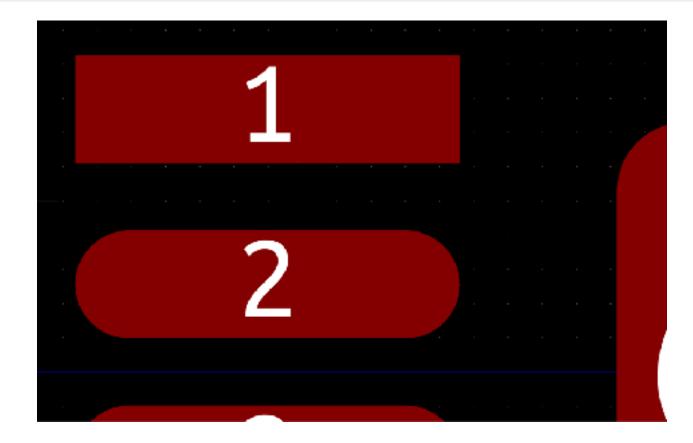




The Case for Rectangular Pin 1

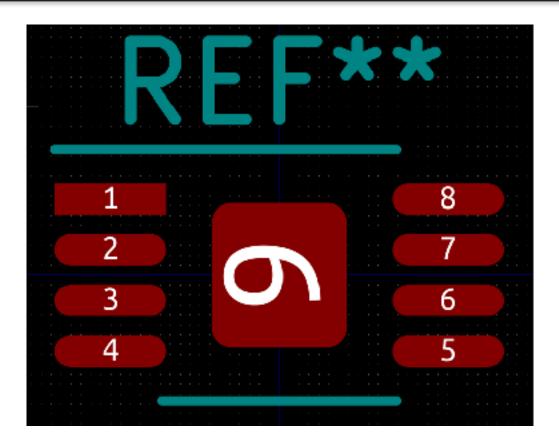
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Gen	eral Local Clearance and	dSettings	Custom Shape Primitives		Footprint REP** (LFCSP-16-1EP_3rSmm_P0.5mm_EP1.8xt.6mm)
Pad number:	1		Hole shape: Circular	0	front side, rotated 0.0 deg
Net name:	<no net=""></no>	×	Hole size X: 0	mm	
Pad type:	SMD		Hole size Yt 🛈	mm	
Shape:	Rounded Rectangle	0			
Shellin .	-1.4375	mm	Copper: F.Cu	0	
Position Y:	-0.75	mm	Technical leyers: F. Adhes B. Adhes F. Paste B. Paste F. SilkS B. SilkS F. Mask B. Mask Dwgs.User Eco1.User Eco2.User		
ize X:	0.826	mm			
ize Y:	0.25	mm			
Orientation:	0.0	🖌 deg			
Shape offset X:	0	mm			
Shape offset Y:	0	mm			
ad to die length:	0	mm			
frapezoid delta:	0	mm			
Trapezold axis:	Vertical	0			
Corner size:	26.0	96			Show pad in outline mode
Comer radius:	0.0626	mm			



Gen	Local Clearance and S	ettings	Custom Shape Primitives		Footprint REF** (LFCSP-16-1EP_3x3mm_P0.5mm_EP1.5x1.6m
Pad number:	a .		Hole shape: Circular	0	front side, rotated 0.0 deg
Net name:	Circular Oval	5	Hole size X: 0	mm	
Pad type:	Rectanguler		Hole size Y: 0	mm	
	Trapezoldal Z Rounded Rectangle	i .			
Position X:	Custom (Circ. Anchor) Custom (Rect. Anchor)	mm	Copper: F.Cu	2	
Position Y:	-0.25	mm	Technical layers: F.Adhes		
Size X:	0.825	mm	F.Aches B.Aches ₽.Paste B.Paste F.SilkS		
Size Y:	0.26	mm			
Orientation:	0.0	deg			
Shape offset X:	0	mm	8.SikS		
Shape offset Y:	0	mm	F.Mask		
Pad to cie length:	D	mm	B.Mask		
Trapezoid delta:	D	mm	Dwgs.User Ecol.User		
Trapezoid axis:	Vertical	5	Eco2.User		-
Corner size:	26.0	N			Show pad in outline mode
Corner radius:	0.0625	mm			

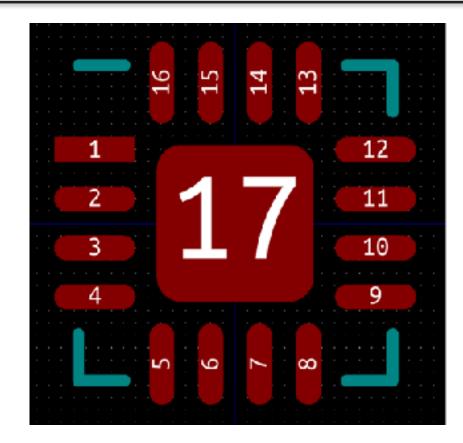


·0.6m

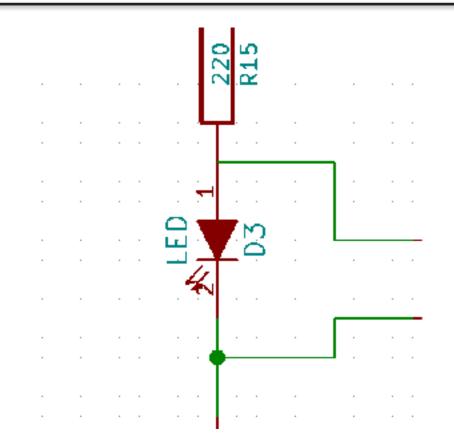


Gen	crai Local Clearance and	Settings	Custom Shape Primitives		Footprint REF** (LFCSP-16-1EP_3x3mm_P0.5mm_EP1.6x1.6mm)
ad number:	ā		Hole shape: Circular	0	front side, rotated 0.0 deg
let name:	Circular Oral		Hole size X: 0	mm	
in the second se	Rectangular Trapezoidal		Hale size Y: 0	mm	
shape: v	Rounded Rectangle		0		
osition X:	Custom (Circ. Anchor) Custom (Rect. Anchor)	mm	Copper: F.Cu		
osition Y:	-0.25	mm	Technical layers:		
áze X:	0.825		F.Adhes B.Adhes ✔ F.Paste B.Paste		
ize Y:	0.25	mm			
		_			<u> </u>
prientation:	0.0	🖌 deg	F.SikS		
hape offset X:	a	mm	B.SikS Z.F.Mask B.Mask Dwgs,User		
hape offset Y:	0	mm			
ad to die length:	0	mm			
		-			
'repezoid delte:	0		Ecol.User		
rapezoi diaxia:	Vertical	0	Eco2.User		-
orner size:	25.0	76			Show pad in outline mode
orner radius:	0.0625	mm			

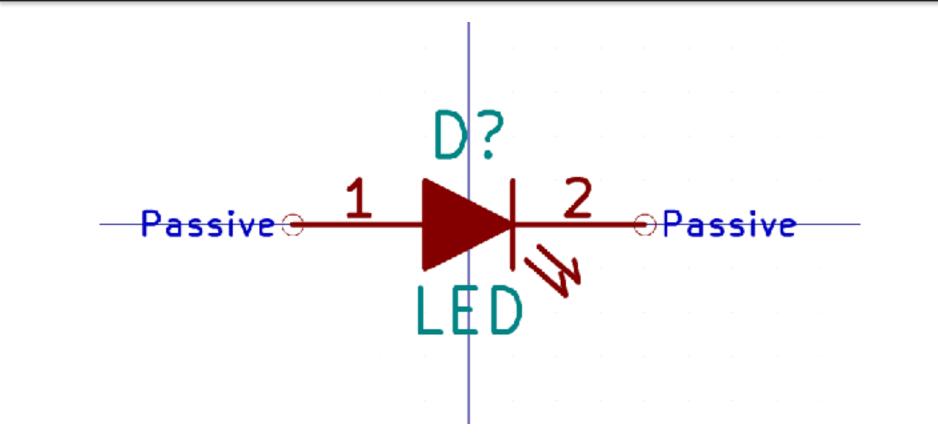




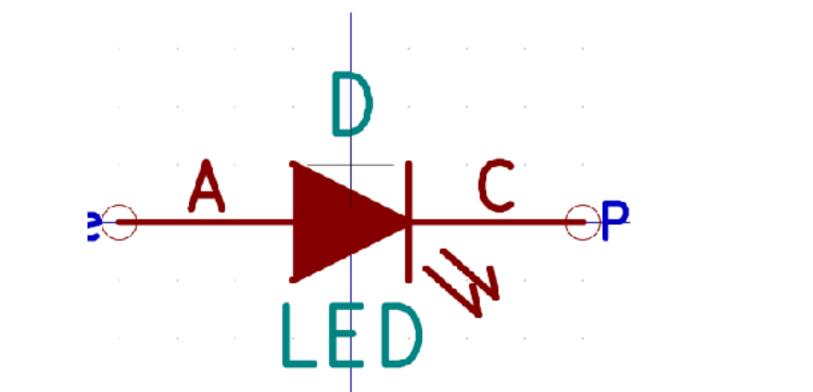














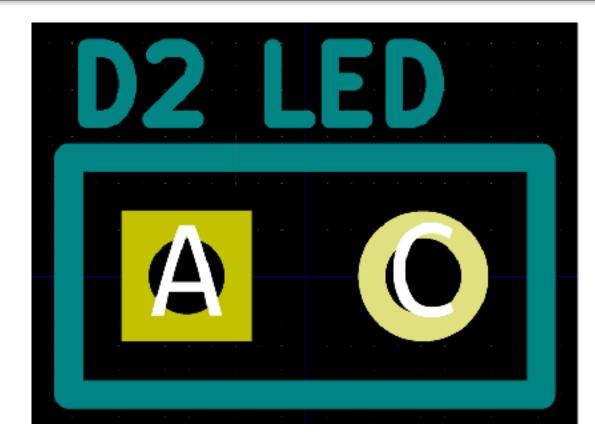


• •		Pin Pro	perties
Pin name:	c		Common to all units in symbol
Pin number:	c		Common to all body styles (DeMorgan)
Electrical type:		~	Visible
Graphic style:	- Line	v	
X position:	5.080	mm	
Y position:	0.000	mm	
Orientation:	┝• Left	•	
Pin length:	3.810	mm	
Name text size:	1.016	mm	
Number text size:	1.016	mm	
			Cancel OK

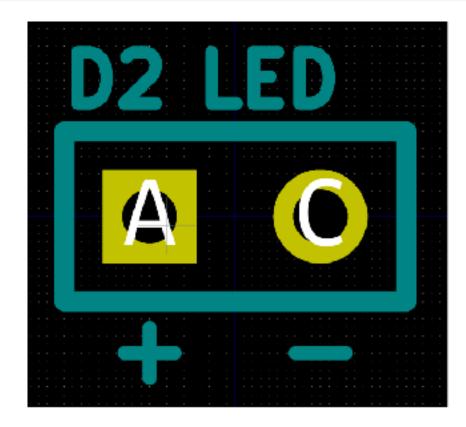
LED Orientation

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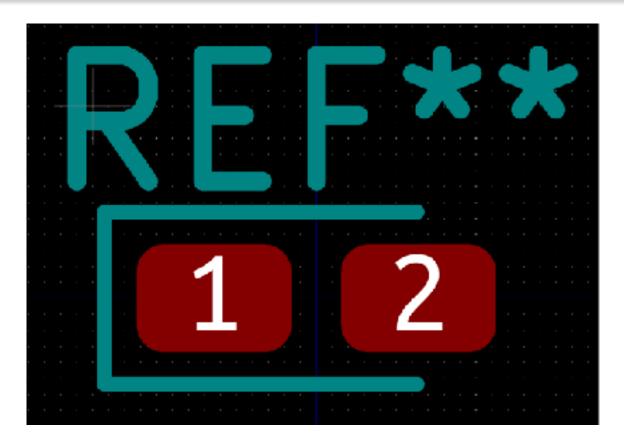




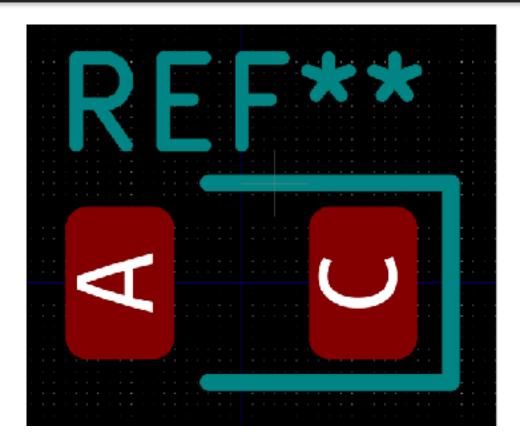






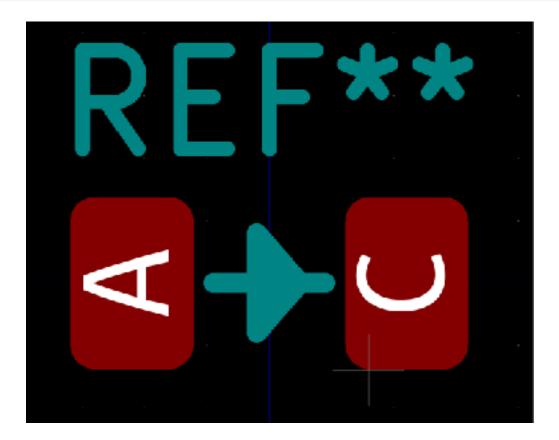






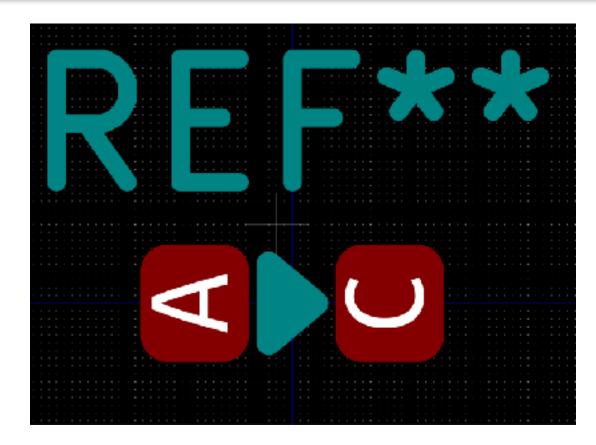
















- 1. Silkscreen pin 1 indicators
 - a. Move them out from underneath the placed part
 - b. Square pad for Pin 1 on IC's
- 2. LED cathode indicators
 - a. Use a C in pin naming scheme
 - b. Use symbol in silkscreen
 - c. Use + and symbols in silkscreen
 - d. Thru-hole: Square pad for Anode. Circle for Cathode

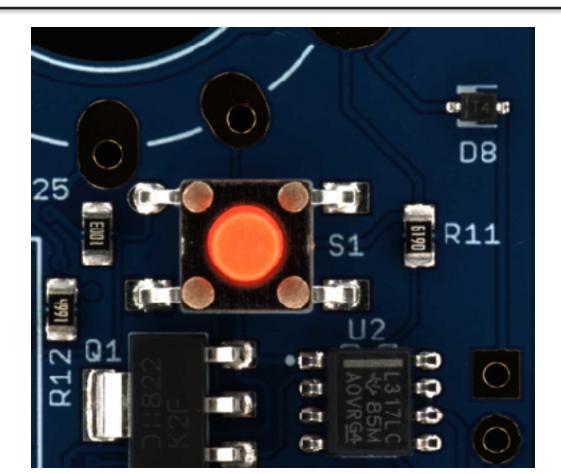




- 1.Identifying polarity of components
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Not minimums









Cozy



Silkscreen Legibility



R2 <u>‡</u> Cozy Text Height 1mm

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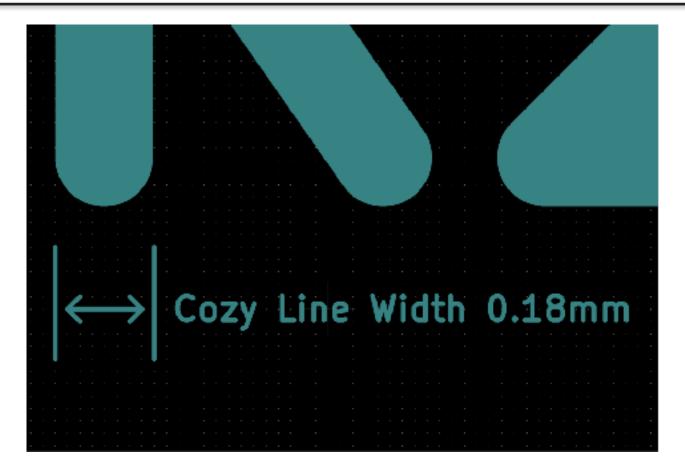
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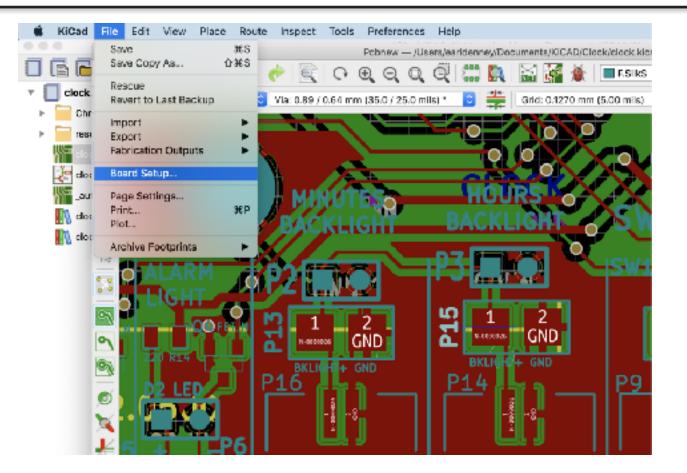
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Silkscreen Legibility



• • •	Board Setup						
▼ Løyers	 Layora Default propersies for new graphic items: 						
		Line Thickness	Tect Width	Text Height	Text Thickness	Italic	Keep Bpright
▼ Design Rules	Silk Layers	0.18 mm	1 mm	1 mm	0.18 mm		2
Net Classes Tracks & Vas	Copper Layers	0.2 mm	1.5 mm	1.5 mm	0.3 mm		2
Solder Mask/Paste	Edge Cute	0.1 mm					
	Courtyards	0.05 mm					
	Other Layers	0.15mm	1 mm	1 mm	0.15 mm		2

Import Settings...

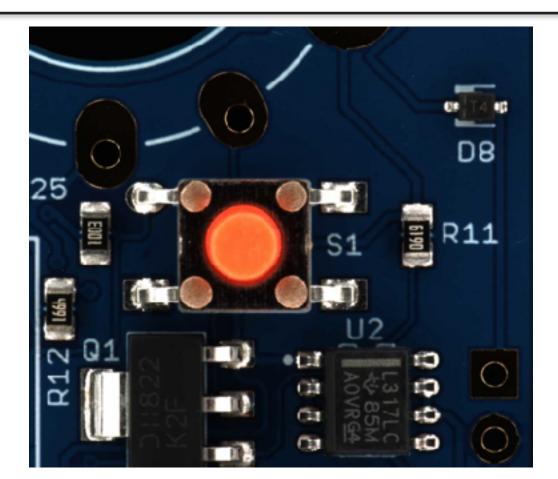




Default properties for new graphic items:								
	Line Thickness	Text Width	Text Height	Text Thickness	Italic	Keep Upright		
Silk Layers	0.18 mm	1 mm	1 mm	0.18 mm				
Copper Layers	0.2 mm	1.5 mm	1.6 mm	0.3 mm				



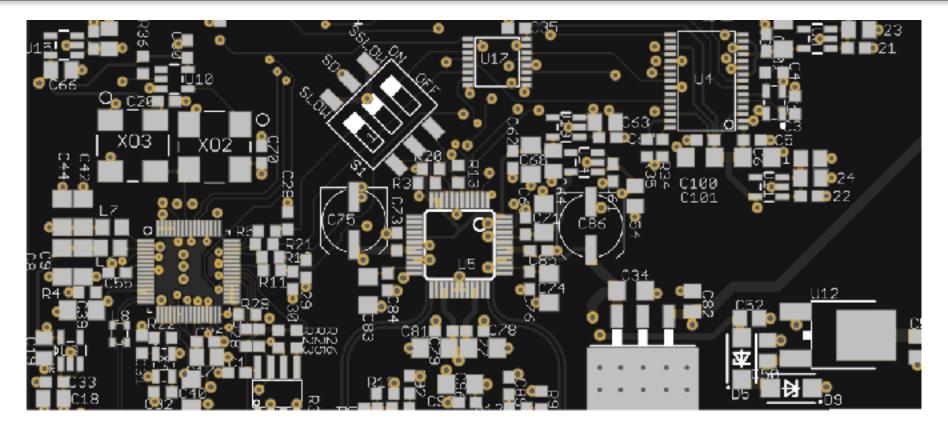






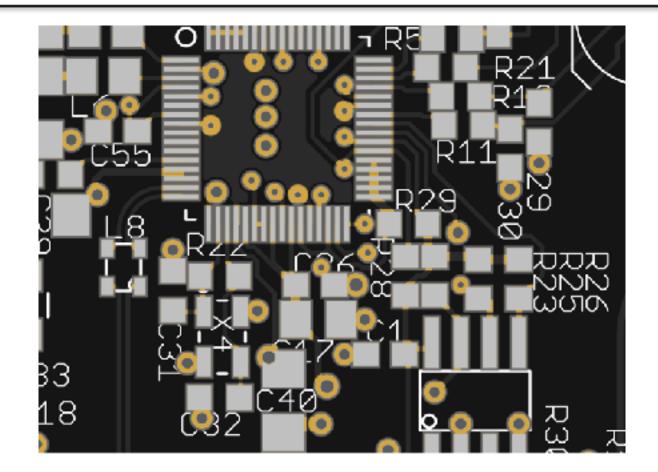
Identifying Polarity





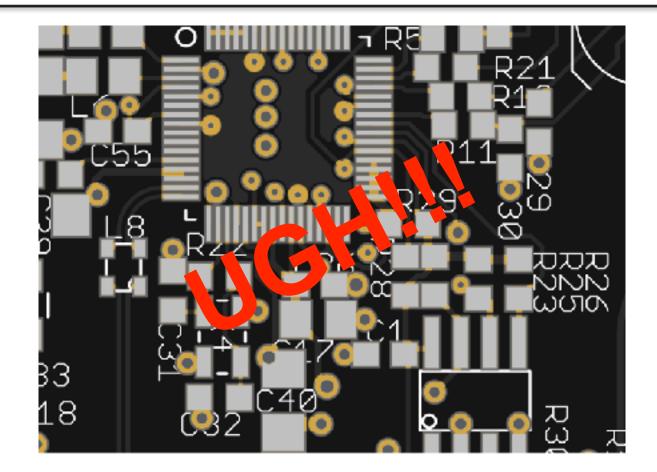






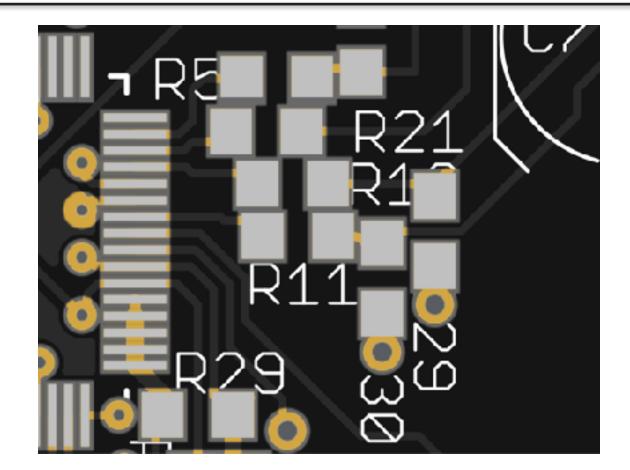






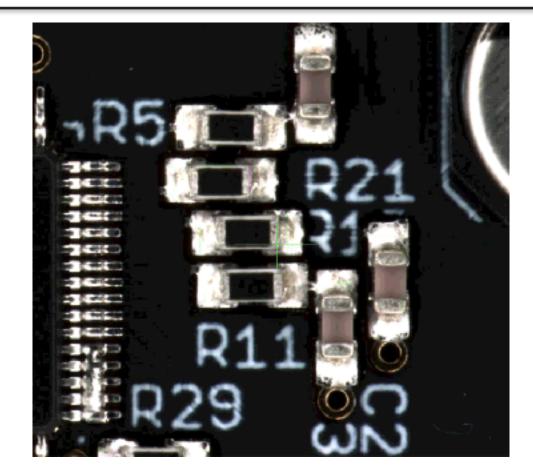






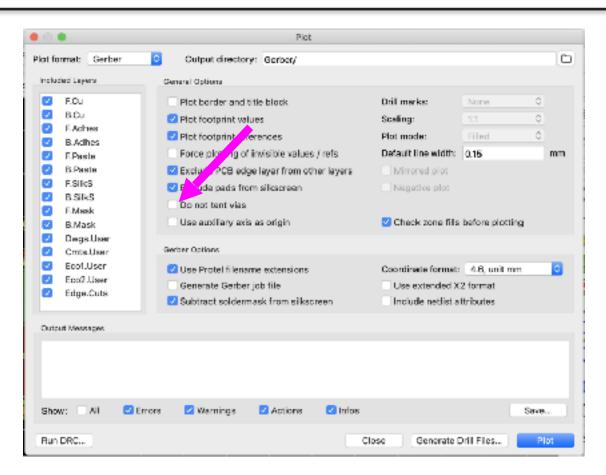






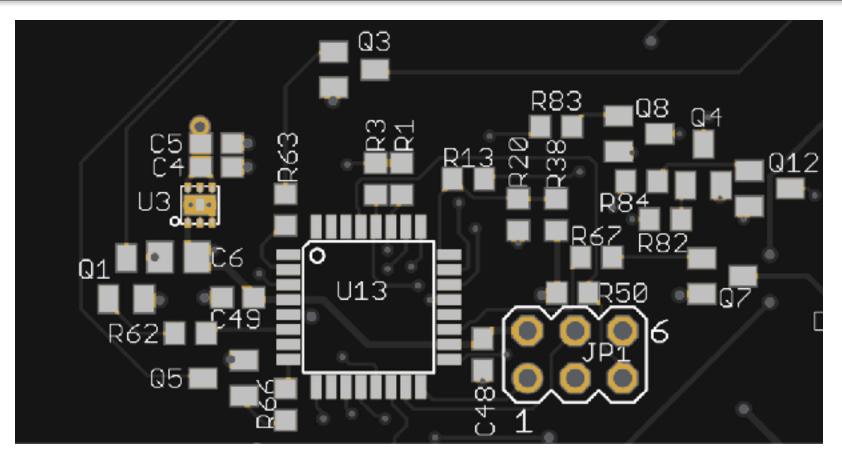






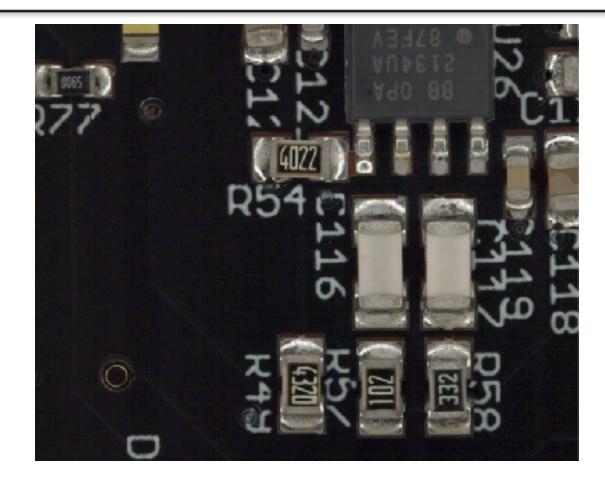






















- 1. Cozy Text: 1x1mm characters and 0.18mm line width
- 2. Move silkscreen away from pads, holes, and vias
- 3. Tent vias to print on top of vias but only if you must

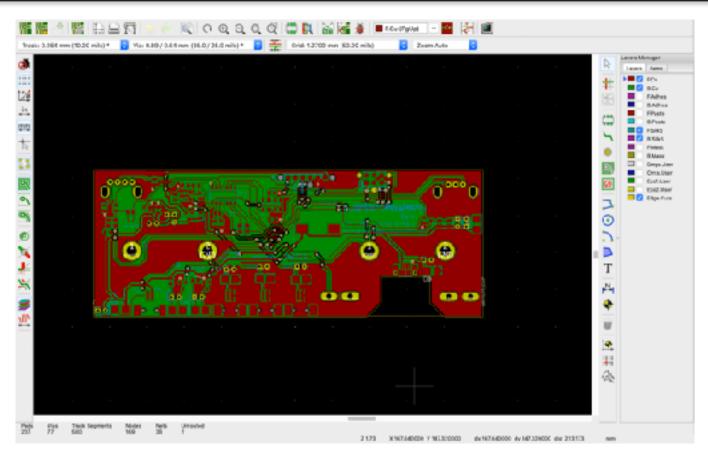




- 1.Identifying polarity of components
- 2. Silkscreen legibility
- **3.**Panelization
- 4.PCB properties
- 5. Specific manufacturer's part numbers

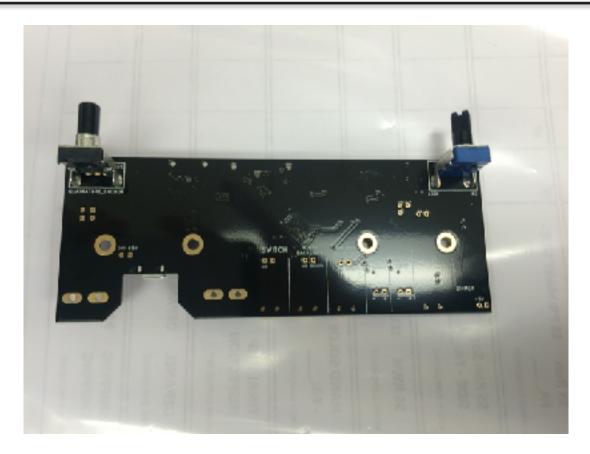








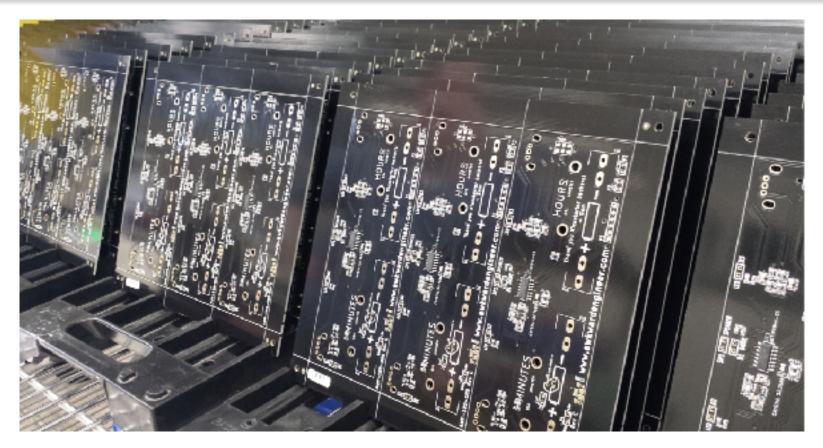






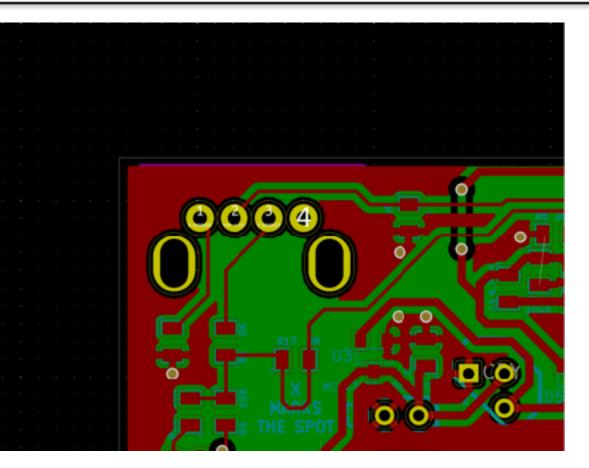












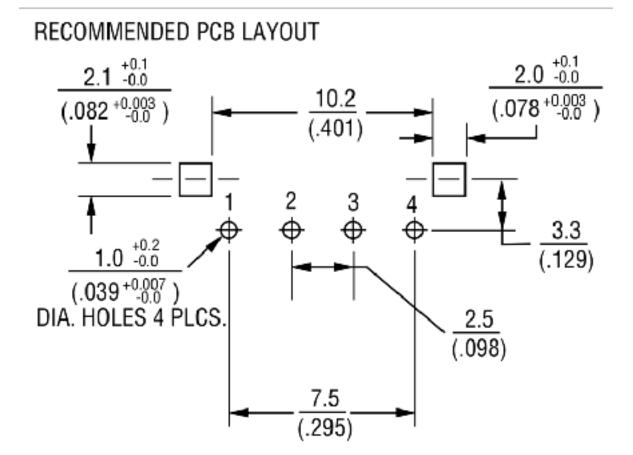




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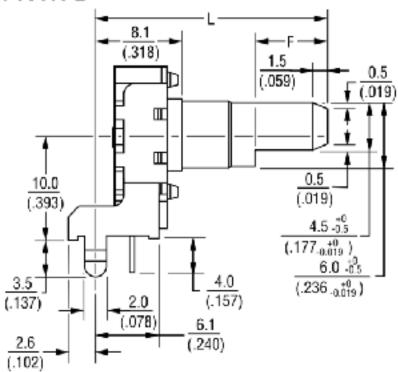






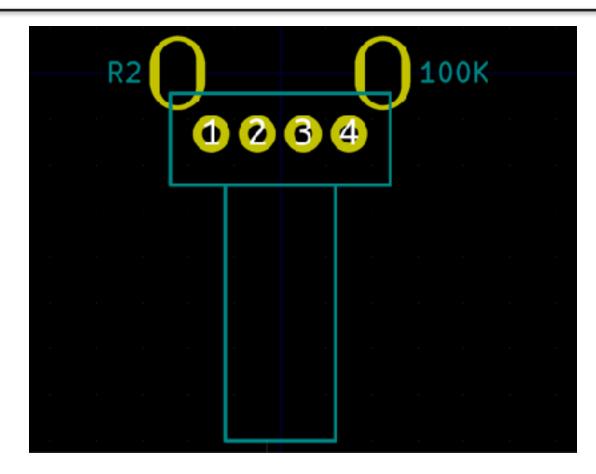


PTV111-2



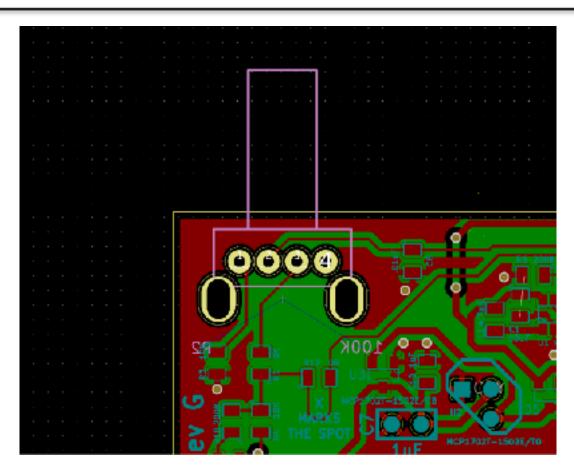






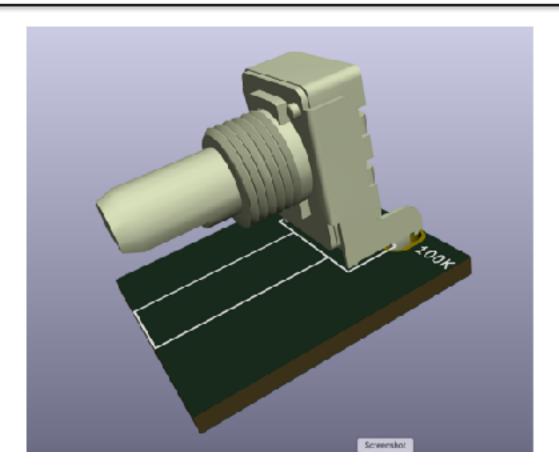






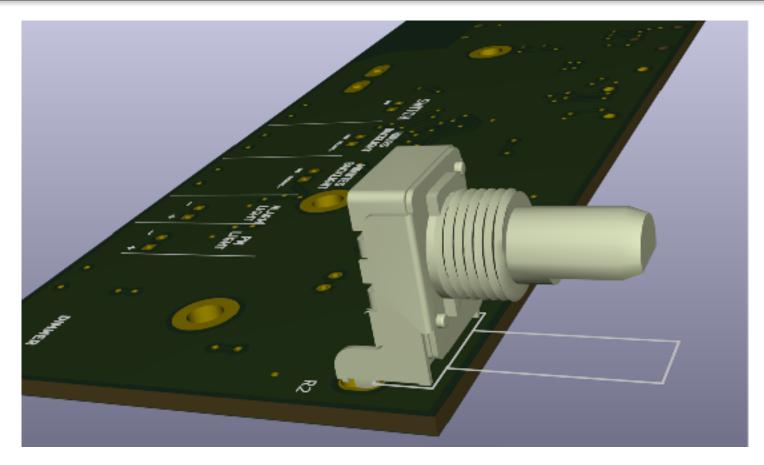
















1. Add silkscreen representing body of component.

- 1.1.Doesn't have to be elaborate, just accurate.
- 1.2.Don't worry, silkscreen that falls outside of the Outline will be trimmed.
- 2. Add 3D Model if you can



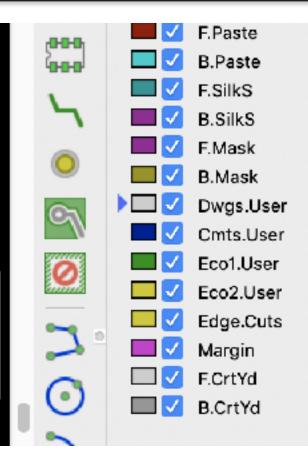


- 1.Identifying polarity of components
- 2. Silkscreen legibility
- 3. Panelization
- **4.PCB properties**
- 5. Specific manufacturer's part numbers



- 1. Number of layers
- 2. Overall PCB thickness
- 3. TG rating
- 4. Inner copper weight
- 5. Outer copper weight
- 6. Silkscreen color
- 7. Soldermask color
- 8. Via-in-pad
- 9. Impedance control
- 10. E-Test Required







• • •		Text Prope	arties	
2. PCB Thio 3. TG Ratin 4. Inner Co 5. Outer Co 6. Silkscree 7. Soldermi 8. Via-In-Pi	pper Weight: 0.5oz apper Weight: 1oz an Color: White ask Color: Green ad: Fill and Plate de Control: Top Layer 2			ar Waveguide 50 ohm
Layer:	Dwgs.User ~			
Width:	3	mm	Italic	
Height:	3	mm	Justification:	Left ᅌ
Thickness:	0.5	mm	Orientation:	0.0
Position X:	25.019	mm	Mirrored	
Position Y:	252.984	mm		
			C	ancel OK



	Paper		Title Block Parameters
Size:			Issue Date
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Height:	279.4	mm	Clock
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	Layout Preview		Comment1
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			Comment2
			Schematic Design: Sam Feller
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			Layout Design: Sam Feller
		_	Comment4
		-	sam@awkwardengineer.com
			Page layout description file
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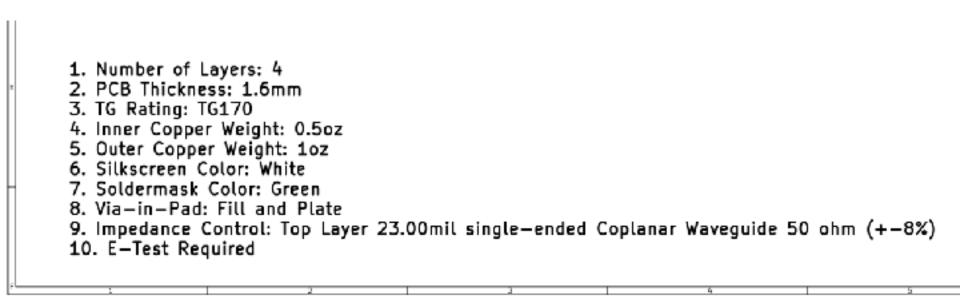




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Ecc1.User Ecc2.User	Z Exclude PCB edge layer from other layers	Mirrored plot		
Edge.Cuts	Exclude pads from silkscreen	Negative plot		
Margin	Do not tent vias			
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sam@awkward	engineer.com			
Layout Design	: Sam Feller			
Schematic Des	sign: Sam Feller			
Please direct	all questions to Sam Fell	ler		
The Awkward B	Engineer			
Sheet:				
File: clock.kic	ad_pcb			
Title: Cloc	k			
Size: A3	Date: 2019-04-09		Rev: A	
KiCad E.D.A.	kicad (5.1.0-0)		ld: 1/1	٦,
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- 1. Number of layers
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Name	Value	Show	H Align	V Align	Italic	Bold	Text Size
Reference	C7		Left	Center			1.016 mm
/alue	1uF		Left	Center			1.016 mm
ootprint	C1		Center	Center			0.762 mm
Datasheet	m		Center	Center			1.524 mm
MPN	CL21B105KAFNNNE		Center	Center			1.270 mm
Vanufacturer	Samsung		Center	Center			1.270 mm
+ 🛧 🖡		Orie	entation	(Update F Asp		om Library
.ibrary Refere Jnit:	C C C C C C C C C C C C C C C C C C C	0	0 +90 +180 -90		- O		around X axis around Y axis

Specific Manufacturer's Part Numbers

VAi



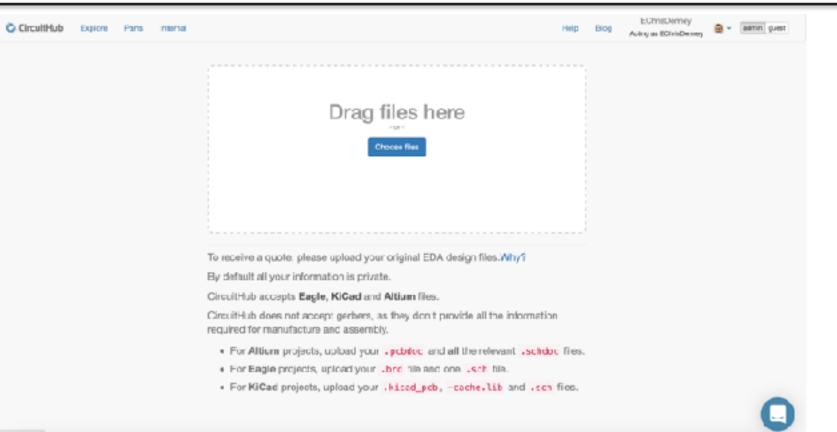
Name	Value	Show	H Align	V Align	Italic	Bold	Text Size
Reference	C7	~	Left	Center			1.0°F.a.m
Value	1uF		Left	Center		+ (l. 16 mm
Footprint	C1		Center	Cente	15		0.762 mm
Datasheet		~	Cen er	L 17 an			1.524 mm
MPN	CL21B105KAFNNNE			Center			1.270 mm
Manufacturer	Samsung	-C 0	Center	Center			1.270 mm
+ ↑ ↓ symbal	CL21B105KAFNNNE Samsung	Orio	entation		Update F Asp		om Library
Library Nofel Unit:	Clock-rescue:C		0 +90 +180 -90		0		around X axis around Y axis



🖸 Group symbols 🛛 🖸	Reference	Value	Footprint	atashe	NPN	Manufacturer	Qty	
	R17	OR	SM0605	-	DNP		1	
Field Show Group By	> R1, R16	OK .	SM0805	~	ERJ-SGEY0R00V	Panasonio	2	
Reference 🧭 🗹 Value 📝 📝	> C2, C4	12.5pF	SM0605	-	CL21C120JB81PNC	Samsung	2	
Fostprint 🗹 🗹	> C6, C6, C8	.01uF	SM0805	AF	CL21B103KBANNNC	Samsung	3	
Detesheet 🔽 🗌	C7	1uF	C1	~	CL21B105KAFNNNE	Samsung	1	
MPN 🗹 🗌	C10	1uF	SM0605	-	CL21B105KAFNNNE	Samsung	1	
Manufacturer 🗹	L1	4.7uH	SM0805	AF	LQM21NN4R7K10L	Murata	1	
	> C1, C3	10 uF	SM0605	-	CL21B106KOQNNNE	Samsung	2	
	> R13-R16	220	SM0805	80 -	ERJ-6GEYJ221V	Panasonio	3	
	 R3, R4, R9, R12 	10K	SM0605	-	RMCF0805FT10K0	Stackpole	4	
	> R7, R8	33K	SM0806		ERJ-6ENF8302V	Panasonio	2	
	> R10, R11	51K	SM0805	~	ERJ-5GEYJ513V	Panasonic	2	
	R2	100K	Chris_Denney_Library:bourns_knob	~	PTV111	Bourns	1	
	RG	130K	SM0806		ERJ-5ENP1303V	Panasonio	1	
	> R8, R18	200K	SM0605	~	ERJ-8ENF2003V	Panasonic	2	
	> DS1, DS2	AMMETER	ammeter		DNP		2	
	IC1	ATTINY84A-SS	SD14E		ATTINY84A-SSU	Microchip	1	
	CON1	AVR-ISP-6	ISPheader		DNP		1	
	> BT1, BT2	BATTERY_CLIP	AA_Battery_Clip_THRU_HOLE_BK-92		92	Keystone	2	
Add Field	> P2-P4, P8, P10	CONN_2	SL-2		DNP		5	



netlist_form_OrcadPcb2	Plugin nickname: bom2grouped_csv
bom2grouped_csv bom2csv bom_with_title_block_2_csv netlist_form_cadstar-RINF netlist_form_pads-pcb.asc bom_csv_sorted_by_ref bom_sorted_by_ref bom_csv_grouped_by_value_with_fp netlist_form_cadstar bom_html_grouped_by_value	Functionality: * Generate a comma separated value BOM list (csv file type). * Components are sorted by ref and grouped by same value+footprint One value per line Fields are Reference, Quantity, Value, Footprint, Datasheet The command line is xsitproc -o "%O.csv" "FullPathToFile/bom2groupedCsv.xsl" "%I"
+ 🖉 🐨	icad.app/Contents/SharedSupport/plugins/bom2grouped_csv.xsl" "%l"



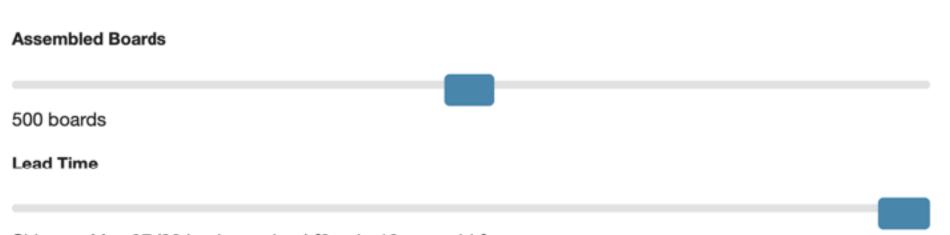


	No website or predival & Revision #12	nk provisiond • 1	New Revision	7 Fe	et 5 ±	Download asse	te	Cad		
	J Parts	> Scherratics	⊘ Board	Firmware	$\bigcirc^{\mathbb{D}}$ Settings					
RDER BY References	-							Q,		
		Part						Quantity	Quantity	Price
BATTERY_CLIP	AA Battery Clp.T.	- 92 Keyatone		BATTERY CO	NTACT CUP A/AA PC P	PEN		1,100 row.or attrition	\$3.1287	\$141.570
10u ^e	346605	C0805C104 Kernet	KSRACTU	CAP GER 0.1	UF SOV KAROBOS			1,850	\$3.0294	\$30.838
ssembled Boards		_				Quantity	Unit Price	Tetal		
0 boards					E PCB	600	\$2.01	\$1,004.16		
ad Time				_	o ¢ Parts	500	\$4.01	\$2,007.36		
nips on May 27 (20 bus	iness days) [5 pck, 10 as	sembly]			ta Assembly	500	\$5.91	\$4,432.77		
					Tctal	500	\$14,93	\$7,464.31 Hide	details	-
							Order			
play a menu										



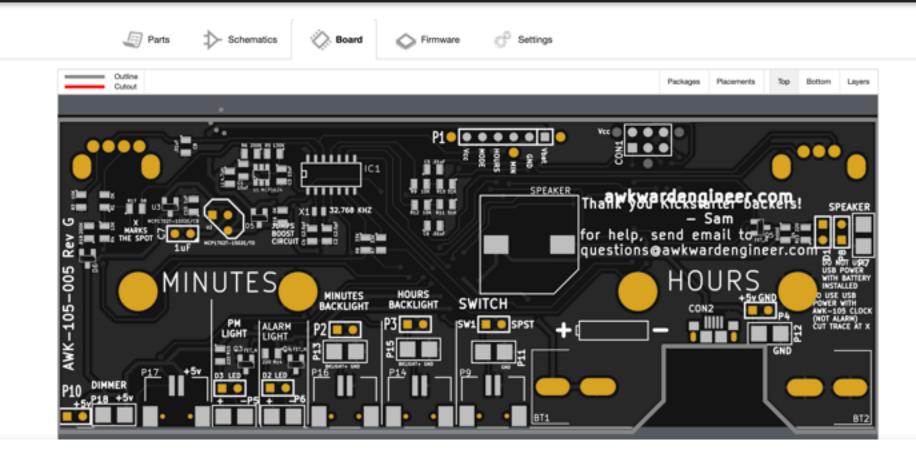
	No website or predival & Revision #12	nk provisiond • 1	New Revision	7 Fe	et 5 ±	Download asse	te	Cad		
	J Parts	> Scherratics	⊘ Board	Firmware	$\bigcirc^{\mathbb{D}}$ Settings					
RDER BY References	-							Q,		
		Part						Quantity	Quantity	Price
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					Tctal	500	\$14,93	\$7,464.31 Hide	details	-
							Order			
play a menu										





Ships on May 27 (20 business days) [9 pcb, 10 assembly]





Specific Manufacturer's Part Numbers

WAi



Color	Stack	kup		
Soldermask color Silkscreen	color Board th	ckness 0		
Black * White	* 1.6			*
	Copper	weight		
	Outer	1 ~ Inner	Not specified *	
Miscellaneous				
Cutouts				
Board does not contain cutouts	Material	 FR4 TG 130-135	TG	
Via fill	Custom	stackup 🕕		
No via fill required				
Add via fill locations	Add	sustom stackup		
Via in pad 0				(2' Edit
No via in pad fill required				
Add locations which require filling and plating	Spec	ifications		
Castellated edges				
Does not require castellated edges	Width		133.35	mm
Blind/Buried layer sets 0	Length		50.81	mm
	Number	of layers	2	





- 1. Include Manufacturer
- 2. Include MPN
- 3. Do this when you assign footprint
- 4. Real legitimate quotes in seconds not days using CircuitHub





- 1. Identifying polarity of components
- 2.Silkscreen legibility
- **3.**Panelization
- 4.PCB properties
- 5. Specific manufacturer's part numbers



- 1.Use square pads or clear silkscreen.
- 2.1x1mm character size. 0.18mm lines.
- 3. Draw overhanging parts
- 4.Include PCB properties in dwgs.User
- 5.Add Manufacturer and MPN to symbols



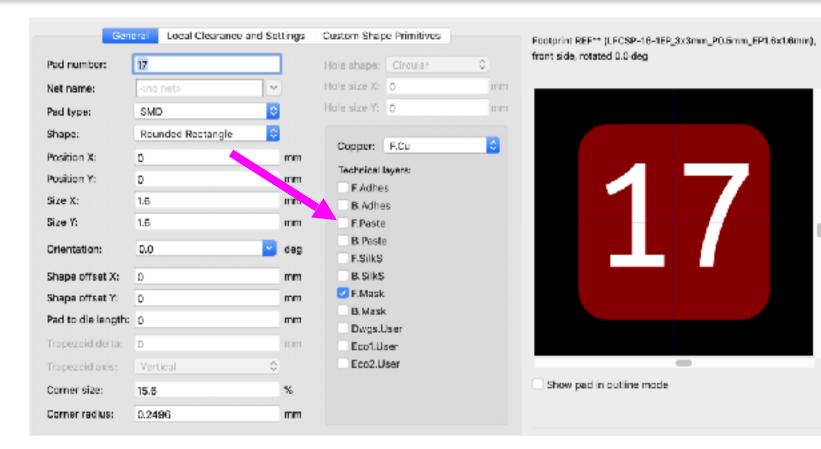


Bonus Tip



Center Pad of QFN/QFP

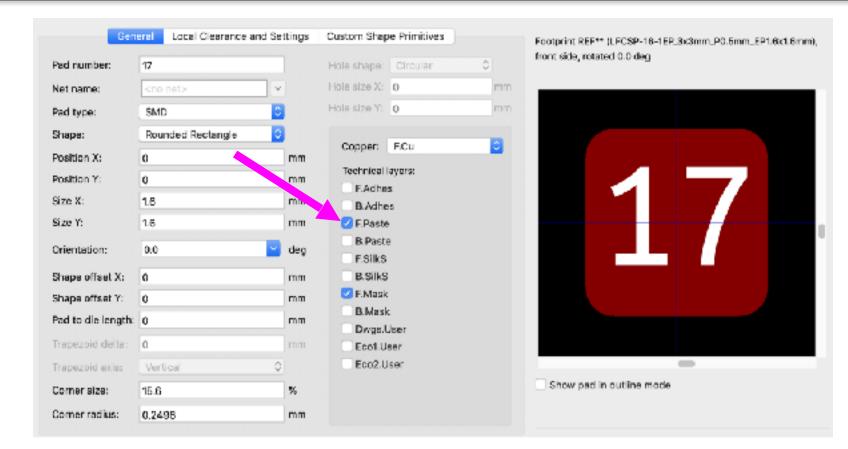






Center Pad of QFN/QFP







Ç.

- Gang soldermask problems
- Plated hole sizes
- Fiducials
- Smallest component sizes
- Single sided vs double sided
- SMT parts being too close to thru-hole
- Cutouts
- Wrong footprints or part numbers
- Your 0402 footprint is probably awful
- Solder paste 1:1 with copper
- Overhanging microUSB ports
- Paste on hybrid components (SMT and Thru-hole in one part)



More Info



More Info worthingtonassembly.com/best-practices

echrisdenney.com





Chris Denney - CTO - Worthington Assembly Inc. Chris Denney - Jerk That Tells You There's a Problem - CircuitHub Inc.

> cdenney@worthingtonassembly.com @WAssembly on Twitter

Thank to Sam Feller (aka The Awkward Engineer) for letting me use his project in this presentation https://www.awkwardengineer.com/